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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/498,677	02/07/2000	Robert Steinhoff	TI-29599	9140

23494 7590 06/11/2007

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
3663	

NOTIFICATION DATE	DELIVERY MODE
06/11/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/498,677	STEINHOFF ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 3/26/07 forms the basis of this office action. In said Amendment Applicants substantially amended claims 1-13 through substantial amendment of independent claim 1 and additionally through substantial amendment of claims 6, 12 and 13. Claims 1-13 are in the application. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. ***Claims 1, 2, 6, 7, 11 and 12*** are rejected under 35 U.S.C. 102(e) as being anticipated by Williamson (6,369,427 B1) (previously made of record).

Williamson teaches a structure (Figures 5-6, col. 6, l. 17 – col. 7, l. 30) comprising:

an external terminal Vdd (e.g., Fig. 5 and col. 5, l. 14);

a reference terminal (ground) (Figure 5 and col. 5, l. 65-66);

a first transistor 56 (col. 6, l. 37-40) formed on a substrate (see jointly Figures 5-6), the first transistor having a current path electrically connected between the external terminal Vdd and the reference terminal (ground) (Figure 5);

a second transistor (p-type transistor in 44) having a current path electrically connected between the substrate (through node 66 and electrical connection with resistor 42 connecting to a terminal common to the two transistors in 44: see Figure 5) (col. 6, l. 17-31);

a third transistor (n-type transistor in 44) having a current path electrically connected between the substrate (through node 66 and an electrical connection with resistor 42 connecting to a terminal common to the two transistors in 44: see Figure 5) and the reference terminal (ground) (see Figure 5) (col. 6, l. 17-31);

wherein the current paths of the second and third transistors are in parallel with the current path of the first transistor (namely: both are connections between Vdd and ground but running as parallel circuitry: see Figure 5).

On claim 2: the structure further comprises a first resistor (either the inherently present contact resistance caused by the contact made between the gate and the source/drain in said second transistor (p-type transistor in 44), or, in an alternative, resistor 42 (N.B.: note that 42 also is located between Vdd (see 46) and said current path of the second transistor) coupled between the external terminal and the current path of the second transistor; and a second resistor coupled between the current path of the third transistor (n-type transistor in 44) and the reference terminal (ground) (said second resistor being either resistor 42 or the contact resistance caused by the contact between the gate of said third transistor and the source/drain terminal closest to ground, respectively).

On claim 6: the first transistor 56 further comprises a control terminal (gate 67) (electrically, in particular: capacitively) coupled to the substrate (col. 6, l. 46).

On claim 7: the structure further comprises a first resistor (either the inherently present contact resistance caused by the contact made between the gate and the source/drain in said second transistor (p-type transistor in 44), or, in an alternative, resistor 42 (N.B.: note that 42 also is located between Vdd (see 46) and said current path of the second transistor) coupled between the external terminal and the current path of the second transistor; and a second resistor coupled between the current path of the third transistor (n-type transistor in 44) and the reference terminal (ground) (said second resistor being either resistor 42 or the contact resistance caused by the contact between the gate of said third transistor and the source/drain terminal closest to ground, respectively).

On claim 11: the structure further comprises a protected circuit 34 (col. 4, l. 27-47) electrically connected to the external terminal Vdd (Figure 5).

On claim 12: the first transistor 56 is a MOS transistor (NMOS transistor; see col. 6, l. 37-40) having a control gate 67 (col.6, l. 44-48) electrically connected to the substrate through capacitive coupling (any MOS transistor is a MOS capacitor and capacitive coupling meets "electrically connected".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 3-5, 8-10 and 13*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Williamson as applied to claim 1 above, in view of Williams (6,060752).

On claims 3-4 and 8: As detailed above, Williamson anticipates claim 1. Williamson does not necessarily teach the further limitations defined by claims 3-4, or claim 8. However, it would have been obvious to include said further limitations in view of Williams, who, in a patent on a semiconductor-based ESD protection circuit (title, abstract), hence analogous art, teaches a lightly doped region as substrate 900, having a first type conductivity (p-type in Williams), a first heavily doped region (NBL region 926 or NBL region 928) having a second conductivity type (n-type in Williams) and underlying the substrate and the active region so as to suppress parasitic capacitance; and a second lightly doped region 904 having second conductivity type (n-type in Williams) formed at a face of the substrate and extending to the first heavily doped region. *Motivation* to include the teaching by Williams in the invention by Williamson derives from the resulting diode (D1) protection through the doping of the substrate, (b) additional protection provided by the well region 904 and (c) the suppression of parasitic capacitance through heavily doped buried region (926 or 928), which are advantages independent of the nature of the device operating through the active region. Note that this motivation holds for any of the transistors in the circuitry by Williamson.

On claim 5: in the combined invention the interface between 62 and 65 on the one hand, and the well region equivalent to 60 on the other hand form first and second

diodes coupled between the external terminal and the second lightly doped region (well region), and between the reference terminal and said second lightly doped region.

On claim 9: in the combined invention the region of substrate 60 is a lightly doped well of conductivity type opposite those of the diffusion regions. Therefore, first and second diodes are formed (60 appropriately modified to be lightly p-doped following Williams) as well as a second terminal 60 coupled between respectively the first and second resistor and the current path (channel) of respectively the second and third transistor (N.B.: all three channels themselves being coupled to each other).

On claim 10: the structure further comprises: an isolation circuit 36 (col. 5, l. 1-5; also col. 4, l. 20-25 and Figure 5) connected to the external terminal Vdd (Figure 5); and a protected circuit 34 (col. 4, l. 26-47 and Figure 5) electrically connected to the isolation circuit.

On claim 13: although Williamson does not necessarily teach the further limitation that the first transistor is a bipolar transistor having a base terminal electrically connected to the substrate, it would have been obvious to include said further limitation in view of Williams, who teach equivalence of MOSFET device based ESD protection circuitry and bipolar transistor based ESD protection circuitry in his invention (see col. 2, l. 50-55).

2. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Williamson as applied to claim 1, in view of Maeda (5,976,921).

As detailed above, claim 1 is anticipated by Williamson. Williamson does not necessarily teach the further limitation defined by claim 13. However, it would have

been obvious also to include said further limitation in view of Maeda, who, in a patent on an semiconductor based ESD protection device (title, abstract), hence analogous art, teaches a ESD protection device based on MOS transistors and a bipolar transistor (see Example 1), wherein a base terminal is electrically connected to the substrate (abstract and col. 13, l. 48-65; P-well being the base; base contact 6aa providing the electrical connection to the substrate: see Figure 8 and col. 14, l. 40-52) so as to enable the escape of excessive current and voltage. *Motivation* to include the teaching by Maeda in this regard derives from the effectiveness of the bipolar transistor to protect against excessive current and voltage.

Response to Arguments

Applicant's arguments filed 3/26/07 have been fully considered but they are not persuasive. Although the rejections are overcome in detail, transistors 52, 56, and 57 being in series rather than in parallel, the claim language does not prevent rejection based on Williamson as cited because the p-type and n-type transistors in voltage clamp 44 meet the claim limitations for second and third transistor, as explained in the rejections overleaf. Furthermore, "electrically connected" does include the case of capacitive coupling.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
June 5, 2007

Primary Patent Examiner:
Johannes Mondt (TC3600/AU3663)